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PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

NISHIKAWA et al.

Serial No.: 10/786,296

Filing Date: February 26, 2004

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE CONFIGURED TO PREVENT THE GENERATION OF A REVERSE CURRENT IN A MOS TRANSISTOR

Customer No. 004372

Confirmation No.: 3437

Art Unit: 2811

Examiner: Ori NADAV

Docket No.: 103213-00072

AMENDMENT UNDER 37 C.F.R. § 1.121

Introductory Comments

Director of the U.S. PTO
P.O. Box 1450
Alexandria, Virginia 22313-1450

June 1, 2005

Sir:

In response to the Office Action dated March 15, 2005, please amend the above-titled application as follows:

Amendments to the claims begin on page 2.

Remarks begin on page 7.